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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/814,141	04/01/2004	Heung-Lyul Cho	0630-1979P	6546

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EXAMINER	
SCHECHTER, ANDREW M	
ART UNIT	**PAPER NUMBER**
2871	

NOTIFICATION DATE	DELIVERY MODE
11/28/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

mailroom@bskb.com

Office Action Summary	Application No.	Applicant(s)	
	10/814,141	CHO ET AL.	
	Examiner	Art Unit	
	Andrew Schechter	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 September 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,15,16 and 20-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,15,16 and 20-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Allowable Subject Matter

1. The indicated allowability of claims 1-4, 15, and 16 is withdrawn in view of the newly discovered reference(s) to *Deane et al.* Rejections based on the newly cited reference(s) follow.

Response to Arguments

2. Applicant's arguments have been considered but are moot in view of the new ground(s) of rejection.

Claim Objections

3. Claim 1 is objected to because of the following informalities: in line 10, "applying a mask in" should be "applying a mask over"; in line 13, "forming a contact hole over" should be "forming a contact hole in". Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-4, 15, 16, and 20-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Deane et al.,* U.S. Patent No. 6,686,229 in view of official notice.

Deane discloses [see Fig. 1, for instance] a fabrication method of a liquid crystal display device, comprising: forming a gate line [5] on a substrate by applying a gate photoresist pattern by printing [col. 7, lines 60-67], sequentially forming a gate insulating layer [13], a semiconductor layer [17], and a high-concentrated N+ layer [19] over the gate line; forming an active region including the high-concentrated N+ layer by applying an active photoresist pattern by printing [col. 7, lines 60-67]; forming a conductive layer [23] over the active region; forming a source/drain electrode [29, 27]; forming a passivation layer [33] over the source/drain electrode; forming a contact hole [35] in the passivation layer by applying a contact hole photoresist pattern [34] by printing [col. 6, lines 17-22], and forming a pixel electrode [37] on the passivation layer by printing a pixel electrode photoresist pattern [col. 7, lines 60-67].

For the steps of forming the gate line, forming the semiconductor layer and N+ layer, and forming the pixel electrode, the reference describes directly printing the layers onto the substrate [as can be seen from the "tails" shown in the figures, for instance]. However, the reference also explicitly states [col. 7, lines 60-67] that these printing processes can be replaced with the process of covering the substrate with the material of the layer, printing a photoresist pattern onto the material, and etching to pattern the layer. The reference also provides motivation to do so, in that it avoids the need to use conventional photolithography to process the photoresists, thus lowering costs while not needing to directly print the layer. The examiner has therefore treated

the relevant claim limitations as explicitly disclosed by the reference, as noted above; alternatively, they could be considered as not disclosed by the particular embodiment of Fig. 1 (and initial discussion thereof), but obvious to one of ordinary skill in the art at the time of the invention due to these teachings of *Deane* [col. 7, lines 60-67]. In either case, these claim limitations are met by *Deane*.

Deane does not explicitly disclose depositing a photoresist layer over the conductive layer, applying a mask over the photoresist layer, performing a lithography process, to thereby form the source/drain electrode. Instead, *Deane* merely states that the conductive layer is "then patterned using conventional photolithography" [col. 5, lines 35-36]. The examiner takes official notice that it was well-known in the art for conventional photolithography to include steps of depositing a photoresist layer over a conductive layer, applying a mask over the photoresist layer, and performing a lithography process. It would have been obvious to one of ordinary skill in the art at the time of the invention to have these steps in the method of *Deane*, motivated by the desire to use conventional photolithographic techniques, having high reliability and precision, to form the source and drain electrodes. Claim 1 is therefore unpatentable.

Considering the additional limitations of claim 20, the N+ layer is an impurity-doped layer, and the conventional photolithography process discussed above includes using the patterned photoresist layer to pattern the conductive layer to form a source and a drain electrode over the active region. All the limitations of claim 20 are therefore met as well, so claim 20 is also unpatentable.

The mask (for patterning the source and drain electrodes) includes a channel region [corresponding to region 24 in Fig. 1c, the region between the source and drain electrodes], so claim 2 is also unpatentable. Since the other steps are done by printing rather than conventional photolithography, the mask applied over the photoresist layer in the step of applying the mask is the only mask applied thoughout the method of the independent claim, so claims 15 and 21 are also unpatentable. As discussed above, the step of forming the gate line includes applying a gate photoresist pattern on the substrate by printing, so claim 22 is also unpatentable. As discussed above, the step of forming the active region includes applying an active photoresist pattern including the impurity-doped layer by printing, so claim 23 is also unpatentable.

Considering the limitations of claims 3 and 16, the examiner takes official notice that roller printing and inkjet printing are known in the art. It would have been obvious to one of ordinary skill in the art to use either as the printing technique in *Deane*, motivated by their being reliable, cost-effective techniques for printing. Claims 3 and 16 are therefore unpatentable.

Considering the additional limitations of claim 4, this is also disclosed by *Deane*, Including defining an active layer [15] by sequentially removing the high-concentrated N+ layer and the semiconductor layer by using the active resist pattern formed by printing as a mask [see Fig. 1b]; removing the active resist pattern [inherent]; sequentially forming a conductive layer and a photoresist layer over the active layer, exposing the photoresist layer, performing a development process, and thereby removing the photoresist layer above a channel region by using the mask including the

channel region pattern, and sequentially removing the conductive layer and the high-concentrated N+ layer above the channel region [see Fig. 1c, col. 6, lines 1-5], so claim 4 is also unpatentable.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andrew Schechter whose telephone number is (571) 272-2302. The examiner can normally be reached on Monday - Friday, 9:00 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Andrew Schechter
Primary Examiner
Technology Center 2800
23 November 2007